AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please add claims 29-31.

1. (ORIGINAL) A method for decoding an input bitstream, comprising the steps of:

(A) generating an intermediate bitstream having an intermediate encoded format by converting said input bitstream having an input encoded format and an input order;

(B) storing said intermediate bitstream in said input order; and

(C) generating an output signal having an output order by decoding said intermediate bitstream.

2. (ORIGINAL) The method according to claim 1, wherein said output order has a different sequence for a plurality of macroblocks than said input order.

3. (ORIGINAL) The method according to claim 1, further comprising the step of:

generating a filtered signal by filtering said output signal.

4. (ORIGINAL) The method according to claim 3, wherein the steps of decoding said intermediate bitstream and filtering said output signal are performed substantially simultaneously.

5. (ORIGINAL) The method according to claim 3, wherein said filtered signal comprises a plurality of macroblocks and said output order comprises a raster order.

6. (ORIGINAL) The method according to claim 1, wherein said input encoded format is un-decodable in an arbitrary sequence.

7. (ORIGINAL) The method according to claim 6, wherein said intermediate encoded format is decodable in said arbitrary sequence.

8. (ORIGINAL) A circuit comprising:

a converter configured to (i) generating an intermediate bitstream having an intermediate encoded format by converting an input bitstream having an input encoded format and an input order;

a memory configured to store said intermediate bitstream in said input order; and

a decoder configured to generate an output signal having an output order by decoding said intermediate bitstream.

9. (ORIGINAL) The circuit according to claim 8, wherein said output order has a different sequence for a plurality of macroblocks than said input order.

10. (ORIGINAL) The circuit according to claim 8, further comprising:

a filter configured to generate a filtered signal by deblock filtering said output signal.

11. (ORIGINAL) The circuit according to claim 10, wherein said filter operates on a picture in said output signal substantially simultaneously with said decoder operating on said picture in said intermediate bitstream.

12. (ORIGINAL) The circuit according to claim 8, wherein said input encoded format comprises a content-adaptive binary arithmetic code format.

13. (ORIGINAL) The circuit according to claim 12, wherein said intermediate encoding format comprises a Huffman format.

14. (ORIGINAL) The circuit according to claim 13, wherein said input order comprises a non-raster order and said output order comprises a raster order.

15. (CURRENTLY AMENDED) A method for encoding an input signal, comprising the steps of:

(A) generating an intermediate bitstream having an input order and an intermediate encoded format by encoding said input signal having said input order; and

(B) generating a reconstructed signal having said input order by filtering said input signal substantially simultaneously with encoding said input signal~~; and~~

~~(C) generating an output bitstream having an output order and an output encoded format by converting said intermediate bitstream~~.

16. (CURRENTLY AMENDED) The method according to claim ~~15~~ 29, wherein said output order has a different sequence for a plurality of macroblocks than said input order.

17. (ORIGINAL) The method according to claim 15, wherein the steps of filtering and encoding substantially simultaneously are performed substantially simultaneously for a row in said input signal.

18. (CURRENTLY AMENDED) The method according to claim ~~15~~ 29, wherein generating said output bitstream ~~step (c)~~ comprises the sub-step of:

generating said output bitstream by reordering a sequence for a plurality of macroblocks in said intermediate bitstream.

19. (ORIGINAL) The method according to claim 15, wherein said reconstructed signal comprises a plurality of macroblocks and said input order comprises a raster order.

20. (CURRENTLY AMENDED) The method according to claim ~~15~~ 29, wherein said output encoded format is un-decodable in an arbitrary sequence.

21. (ORIGINAL) The method according to claim 20, wherein said input encoded format is decodable in said arbitrary sequence.

22. (CURRENTLY AMENDED) A circuit comprising:

an encoder configured to generate an intermediate bitstream having an input order and an intermediate encoded format by encoding said input signal having said input order; and

a filter configured to generate a reconstructed signal having said input order by filtering said input signal substantially simultaneously with encoding said input signal~~; and~~

~~a converter configured to generate an output bitstream having an output order and an output encoded format by converting said intermediate bitstream~~.

23. (CURRENTLY AMENDED) The circuit according to claim ~~22~~ 30, wherein said output order has a different sequence for a plurality of macroblocks than said input order.

24. (CURRENTLY AMENDED) The circuit ~~method~~ according to claim 22, wherein said filter and said encoder operate on a picture in said input signal substantially simultaneously.

25. (ORIGINAL) The circuit according to claim 22, wherein said filter comprises a deblocking filter.

26. (CURRENTLY AMENDED) The circuit according to claim ~~22~~ 30, wherein said output encoded format comprises a content-adaptive binary arithmetic coded format.

27. (CURRENTLY AMENDED) The circuit according to claim ~~26~~ 22, wherein said intermediate encoding format comprises a Huffman format.

28. (CURRENTLY AMENDED) The circuit according to claim ~~27~~ 30, wherein said output order comprises a non-raster order and said input order comprises a raster order.

29. (NEW) The method according to claim 15, further comprising the step of:

generating an output bitstream having an output order and an output encoded format by converting said intermediate bitstream.

30. (NEW) The circuit according to claim 22, further comprising a converter configured to generate an output bitstream having an output order and an output encoded format by converting said intermediate bitstream.

31. (NEW) The circuit according to claim 8, wherein said input encoded format is un-decodable in an arbitrary sequence.